DATA SHEET

TDA3592A
SECAM-PAL transcoder

Product specification
File under Integrated Circuits, IC02

January 1988

Philips Semiconductors

PHILIPS

GENERAL DESCRIPTION

The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V:
  $\overline{\text{SECAM}}$ processing shuts down but
  $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9\text{-}1(p\text{-}p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		$V_{4\text{-}1}$	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		$V_{4\text{-}1}$	0	–	2,9	V
Identification at pin 6		$V_{6\text{-}1}$	–	10,6	–	V
Slicing level reference voltage (pin 5)		$V_{5\text{-}1}$	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		$V_{19\text{-}1}$	–	1,5	–	V
Horizontal blanking level		$V_{19\text{-}1}$	–	3,5	–	V
Burst gating level		$V_{19\text{-}1}$	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16\text{-}1(p\text{-}p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		$G_{16\text{-}15}$	–	7,0	–	dB

PACKAGE OUTLINE

24-lead DIL; plastic with heat spreader (SOT-101B); SOT101-1; 1996 November 25.

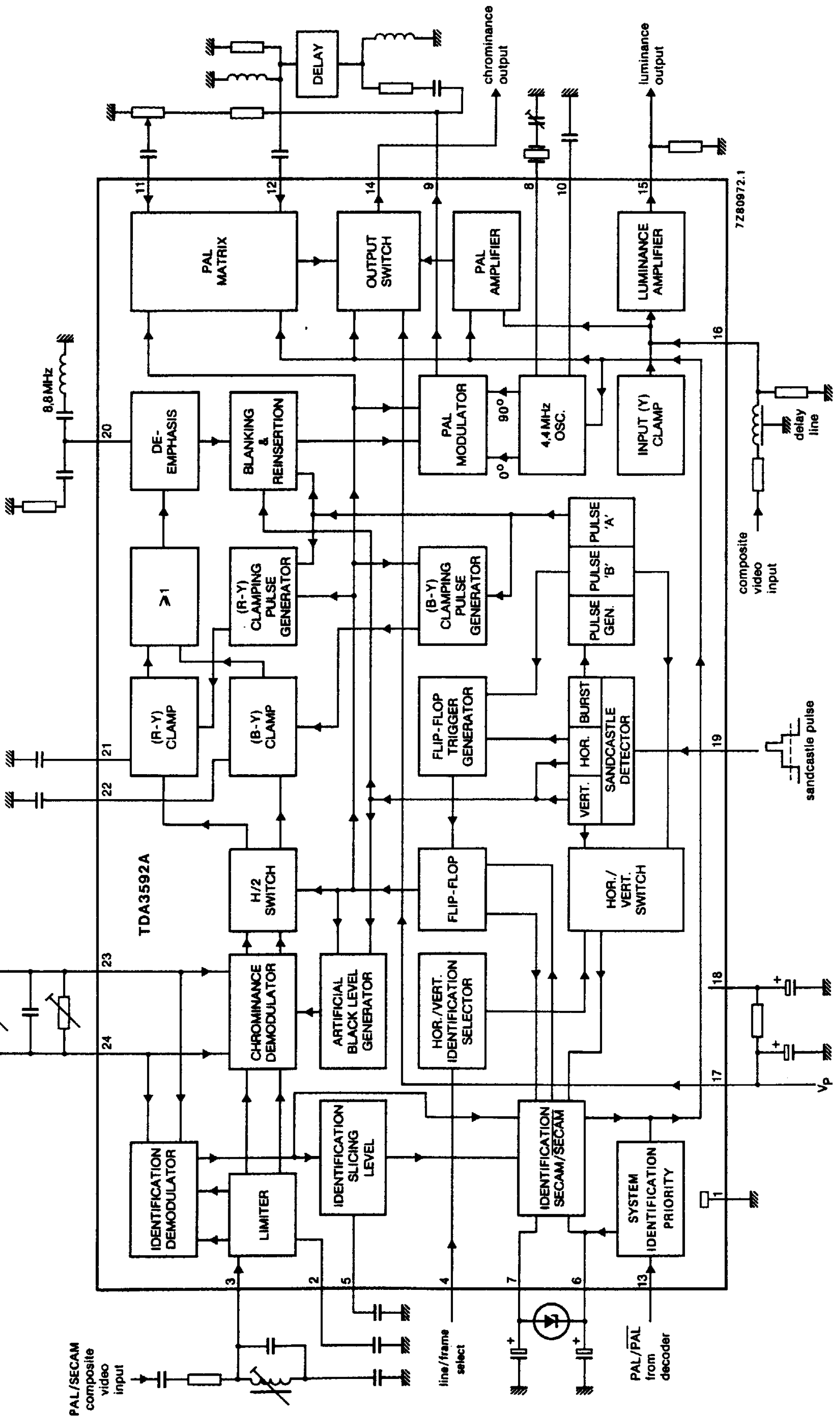


Fig.1 Block diagram.

PINNING

1. Ground.
2. Limiter feedback.
3. Limiter input: chrominance input SECAM; identification input SECAM/$\overline{\text{SECAM}}$.
4. Identification selection input using a DC level to preset the identification mode.
   At V_4< 2,9 V the TDA3592A is preset for frame identification.
   At V_4 > 4,1 V the TDA3592A is preset for line identification.
5. Storage capacitor input for floating level identification.
6. Storage capacitor input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
7. Double time-constant input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
8. 4,43 MHz oscillator.
9. Sequentially modulated output.
10. Decoupling capacitor for miller integrator feedback circuit.
11. Direct input chrominance signal.
12. Delayed input chrominance signal.
13. PAL/$\overline{\text{PAL}}$ input signal from PAL decoder.
14. Chrominance output signal.
15. Luminance output signal.
16. Luminance/$\overline{\text{SECAM}}$ input signal.
17. Positive supply voltage (V_p).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection: R = 560 Ω; C = 1 nF.
21. Storage capacitor connection for (R–Y) clamp.
22. Storage capacitor connection for (B–Y) clamp.
23. Demodulator reference tuned circuit: nominal frequency = 4,33 MHz; nominal Q_L = 2,45.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizontal blanking periods. This is done because of the possibility of horizontal burst signals not being available. The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and –(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180° out of phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse ‘B’ (see Fig.2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4\text{-}1} < 2{,}9$ V;
- Vertical identification preset when $V_{4\text{-}1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse ‘A’ and pulse ‘B’ (see Fig.2). Pulse ‘A’ is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse ‘B’ times the SECAM horizontal identification.

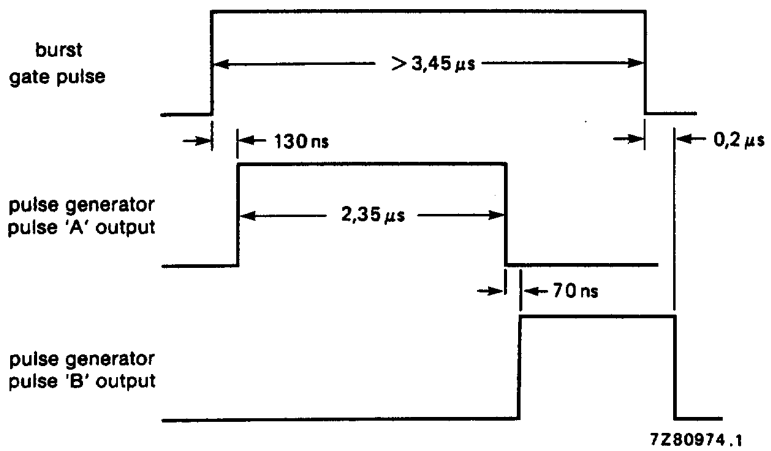


Fig.2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90° phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the –(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 µs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching	During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.
PAL	The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.
SECAM	The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of < 1,1 V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).
Black-and-white	The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL DECODER MODE	SYSTEM OPERATING MODE
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 16 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	–25	+70	°C
Storage temperature range	T_{stg}	–25	+150	°C

CHARACTERISTICS

$V_P = V_{17-1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	µA
Decoupled supply voltage (pin 18)	$R_{ext17-18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	µF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j-a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p-p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p-p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		R_{23-24}	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		C_{23-24}	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Linearity of (B-Y) demodulation (pin 20)	note 3	–	–	94	–	%
Linearity of (R-Y) demodulation (pin 20)	note 4	–	–	100	–	%
(R-Y)/(B-Y) ratio (pin 20)		–	–	1,78	–	%
Relative deviation of reinserted black level/demodulated black level (pin 20) as a function of temperature						
(R-Y) signals	note 5	–	–	0,22	–	kHz/°C
(B-Y) signals	note 5	–	–	0,22	–	kHz/°C
Identification SECAM/$\overline{\text{SECAM}}$	note 6					
Input voltage for line identification (pin 4)		V_4	4,1	–	V_P	V
Input voltage for frame identification (pin 4)		V_4	0	–	2,9	V
Switching level for line/frame identification (pin 4)		V_4	3,0	3,5	4,0	V
Input current (pin 4)		$-I_4$	–	5	25	μA
Voltage at pin 6 during $\overline{\text{SECAM}}$/$\overline{\text{PAL}}$		V_6	–	10,2	–	V
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	11,5	–	V
Voltage at pin 6 during SECAM		V_6	–	7,0	–	V
Identification at pin 6		V_6	–	10,6	–	V
Colour OFF for SECAM		V_6	9,8	10,1	10,4	V
Colour ON for SECAM		V_6	8,8	9,1	9,4	V
Slicing level reference voltage (pin 5)		V_5	–	8,4	–	V
Sandcastle pulse detector and clamping pulse generator						
Voltage level at which the vertical blanking pulse is separated		V_{19}	1,0	1,5	2,0	V
Voltage level at which the horizontal blanking pulse is separated		V_{19}	3,0	3,5	4,0	V
Voltage level at which the burst gating pulse is separated		V_{19}	6,5	7,0	7,5	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input current	V_{19} = 0 V	$-I_{19}$	–	30	100	μA
Width of pulse ‘A’ (Fig.2)	note 7		1,85	2,35	2,85	μA
Required width of pulse ‘B’ (Fig.2)	note 7		0,6	–	–	μs
Luminance amplifier						
Input signal (peak-to-peak value) (pin 16)		$V_{16(p-p)}$	–	1,2	1,7	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,5	7,5	8,5	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		Z_{15}	–	20	–	Ω
Frequency response at –3 dB (pin 15 and 16)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	6,0	7,0	8,0	dB
Frequency response at –3 dB (pin 14 and 16)		f	6,0	–	–	MHz
External load resistance (pin 15)		R_L	2,0	–	–	kΩ
Limiter, chrominance demodulator and PAL modulator	note 8					
Output resistance (pin 9)		R_9	–	25	–	Ω
DC output voltage during horizontal blanking (pin 9)		V_9	–	9,6	–	V
Internal biasing resistor for emitter follower (pin 9)			–	9,0	–	kΩ
External load resistance (pin 9)		$R_{L(9)}$	2	–	–	kΩ
Output signal (pin 9) when input to pin 3 has a Δf of 280 kHz; without external load (peak-to-peak value)		$V_{9(p-p)}$	–	0,82	–	mV
(R-Y)/(B-Y) ratio (pin 9)			1,50	1,78	2,11	
Chrominance/burst ratio for SECAM (pin 9)			2,5	3,0	3,5	
Linearity of (B-Y) signal (pin 9)	note 3		85	92	99	%
Linearity of (R-Y) signal (pin 9)	note 4		93	100	107	%
Black level shift as a function of temperature (pin 9)						
(R-Y) signals	note 9		–	0,22	–	kHz/°C
(B-Y) signals	note 9		–	0,22	–	kHz/°C

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Phase relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			87	90	93	deg
Amplitude relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			–1,5	0	+1,5	dB
Black level shift as a function of supply voltage (pin 9)						
(R-Y) signal			–	–1,5	–	kHz/V
(B-Y) signal			–	1,0	–	kHz/V
Oscillator						
Oscillator frequency (pin 9) (set with series capacitor)		f_{OSC}	–	4,433619	–	MHz
Frequency deviation without spread of external components (pin 9)		Δf_{OSC}	–	–	±150	Hz
Temperature coefficient of oscillator frequency (pin 9)			–	–2	–3	Hz/°C
Frequency deviation for change of V_P from 9,0 to 13,2 V		Δf_{OSC}	–	–	150	Hz
DC voltage (pin 8)		V_8	–	4,7	–	V
Input resistance (pin 8)		R_8	–	1	–	kΩ
DC voltage (pin 10)		V_{10}	–	4,4	–	V
Input resistance (pin 10)		R_{10}	–	2	–	kΩ
PAL matrix						
Input resistance (pin 11)		R_{11}	700	900	1100	Ω
Input resistance (pin 12)		R_{12}	700	900	1100	Ω
Output resistance (pin 14) (SECAM/$\overline{\text{SECAM}}$)		R_{14}	–	40	–	Ω
Internal emitter follower load resistance (pin 14)		$R_{INT(14)}$	–	7	–	kΩ
External load resistor (pin 14)		$R_{L(14)}$	2,4	–	–	kΩ
DC voltage (pin 11)		V_{11}	–	5,0	–	V
DC voltage (pin 12)		V_{12}	–	5,0	–	V
DC voltage (pin 14)	SECAM mode	V_{14}	–	6,2	–	V
DC voltage (pin 14)	$\overline{\text{SECAM}}$ mode and line blanking	V_{14}	–	4,9	–	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
H/2 ripple on chrominance output (pin 14) (peak-to-peak value)	SECAM mode	$V_{14(p\text{-}p)}$	–	–	100	mV
Gain A; pin 11 to 14		G_A	9	10	11	dB
Gain B; pin 12 to 14 ((R-Y) at pin 9)		G_B	9	10	11	dB
Gain C; pin 12 to 14 ((B-Y) at pin 9)		G_C	9	10	11	dB
Gain A – gain B		$G_A – G_B$	–0,7	–	+0,7	dB
Gain A – gain C		$G_A – G_C$	–0,7	–	+0,7	dB
Gain B – gain C		$G_B – G_C$	–0,7	–	+0,7	dB
Phase A; pins 11, 14 to pins 12, 14 ((R-Y) at pin 9)			–	181,5	–	deg
Phase B; pins 11, 14 to pins 12, 14 ((B-Y) at pin 9)			–	1,5	–	deg
Phase A – phase B			178	180	182	deg
Identification PAL/$\overline{\text{PAL}}$						
Input condition for PAL (pin 13)		V_{13}	1,7	–	V_P	V
Input condition for $\overline{\text{PAL}}$ (pin 13)		V_{13}	–	–	1,1	V
Input current	V_{13} = 6 V	I_{13}	–	–	10	µA
Input resistance	V_{13} = 8,2 V	R_{13}	7,5	11,5	15,5	kΩ
Pin 6 internal current in PAL/$\overline{\text{SECAM}}$ mode		$–I_6$	0,24	0,4	0,58	mA
Switching level PAL/$\overline{\text{PAL}}$ (pin 13)		V_{13}	1,2	1,4	1,6	V

CHARACTERISTICS AT LOW SUPPLY VOLTAGE

$V_P = V_{17-1} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supplies						
Supply current		$I_{17}+I_{18}$	16	20	24	mA
Supply voltage switching level for preset SECAM signal path	SECAM processing OFF	V_{17-1}	6,5	7,5	8,2	V
Luminance amplifier						
Input signal (peak-to-peak value)		$V_{16(p-p)}$	–	0,45	0,56	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,0	7,0	8,0	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	µA
Output impedance (pin 15)		$\|Z_{15-1}\|$	–	20	–	Ω
Minimum load resistance (pin 15)		R_L	2	–	–	kΩ
Frequency response at –3 dB (pin 16 to 15)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	5,7	6,8	7,9	dB
Frequency response at –3 dB (pin 16 to 14)		f	6	–	–	MHz

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a) Supply a SECAM signal input to pin 3 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b) Align the reference tuned circuit so that the output signal from pin 14 to the PAL decoder is minimum during scan (PAL black colour information).
2. When the input signal to the limiter (pin 3) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz; f = 4,33 MHz (typ.).
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz.
5. The parameter value is equated by: $\frac{(B-D)/F-(A-C)/E}{Y-X} \times \frac{\Delta f\,(kHz)}{°C}$

   $E = \frac{E1-E2}{2}$ $\qquad F = \frac{F1-F2}{2}$

   Where

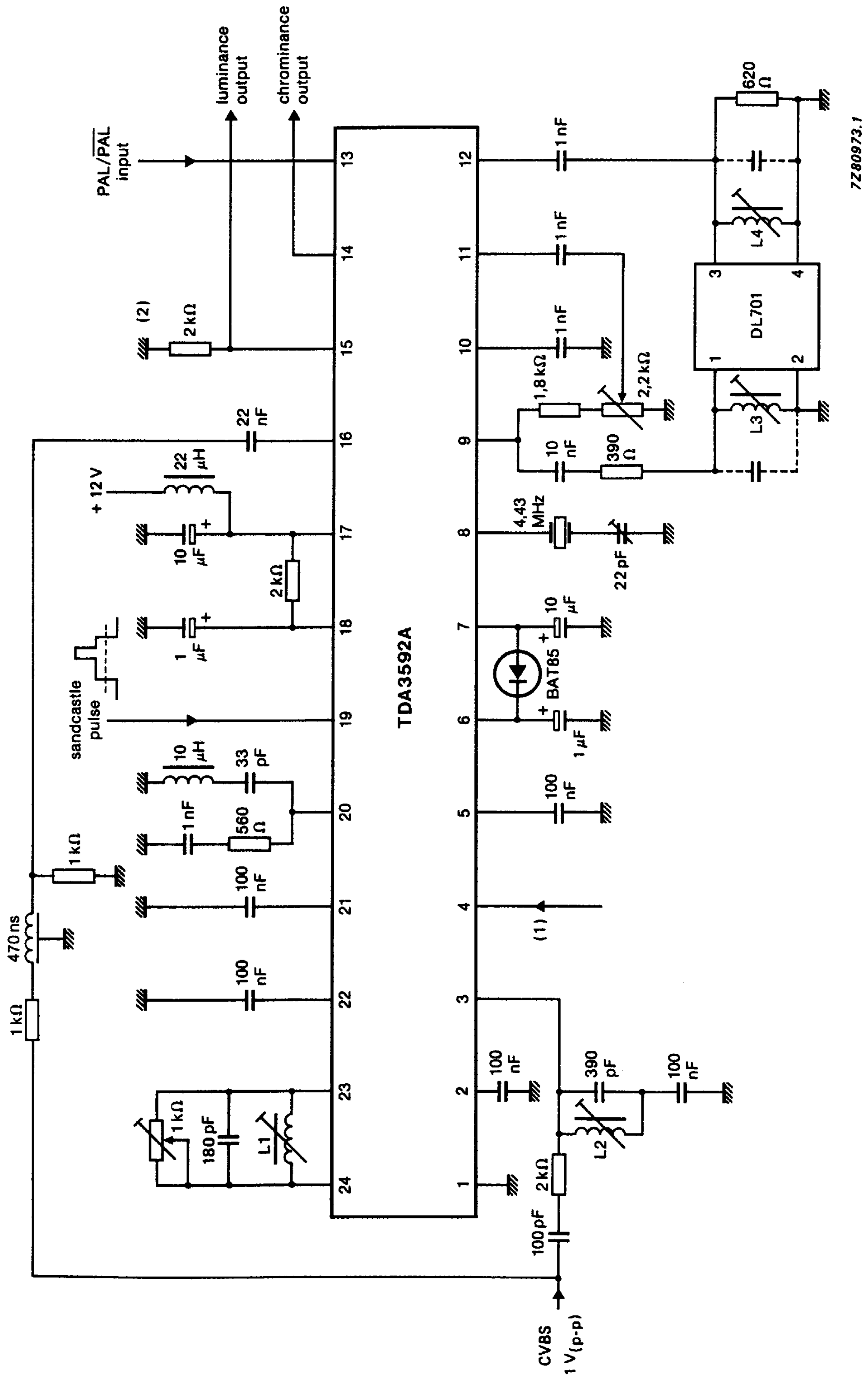
   A = demodulated black level at temperature X
   B = demodulated black level at temperature Y
   C = artificial black level at temperature X
   D = artificial black level at temperature Y
   E1 = demodulated output signal at temperature X ($f_o - \Delta f$)
   E2 = demodulated output signal at temperature X ($f_o + \Delta f$)
   F1 = demodulated output signal at temperature Y ($f_o - \Delta f$)
   F2 = demodulated output signal at temperature Y ($f_o + \Delta f$)
   for B-Y: $f_o = f_{ob}$ = 4,25 MHz (Δf = 230 kHz)
   for R-Y: $f_o = f_{or}$ = 4,40625 MHz (Δf = 280 kHz)

6. During stable signal conditions V_7 is always at V_F (BAT85) below V_6.
7. The burst gate pulse width $> 3{,}45\ \mu s$.
8. The specification figures are only valid when the reference tuned circuit is aligned as indicated in note 1.
9. Ensure that the 4,433 MHz carrier is in the correct phase; black level shift at temperature X = A and at Y = B. Output signal (Δf = 230 kHz for B-Y; Δf = 280 kHz for R-Y) at temperature X = E and at Y = F.

   The parameter is equated by: $\frac{[B/(F-B)]-[A/(E-A)]}{Y-X} \times 230;\ 280\ kH$
10. Chrominance definition – burst ratio at SECAM condition (pin 9).

    The parameter is equated by: $\frac{V_{out\,(p-p)}\,Red\,(R-Y)}{V_{burst\,(p-p)}\,(R-Y)}$.

APPLICATION INFORMATION



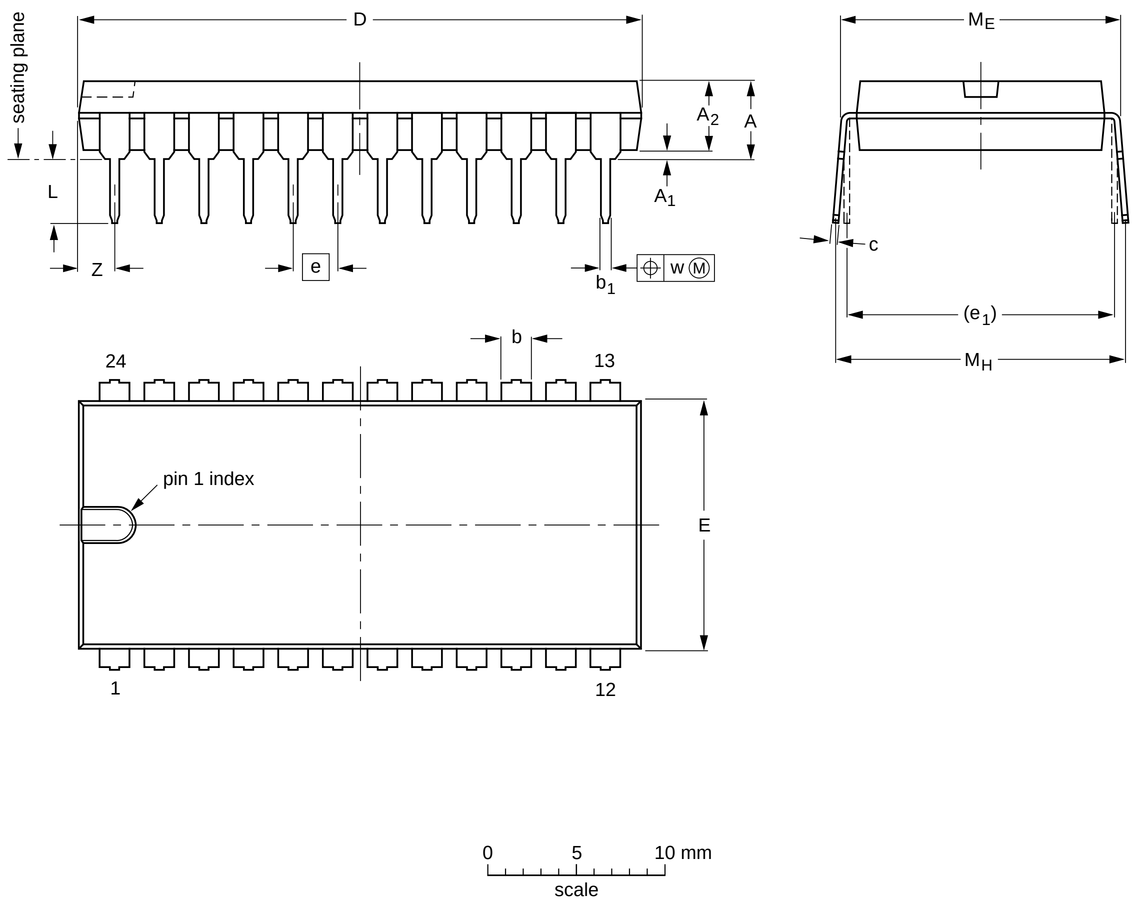
(1) V_{4-1} = sandcastle = line + frame identification
V_{4-1} = ground = frame identification
V_{4-1} = V_P = line identification

(2) minimum load resistance at pin 15 = 2 kΩ

Fig.3 Application circuit.

PACKAGE OUTLINE

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.